MCS6532 DESIGN SPECIFICATION

This specification contains a detailed description of the MOS Technology, Inc. MCS6532. This document is intended to serve as the basis for internal design work as well as a basis for external specifications, manuals, etc.

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MCS6532 DESIGN SPECIFICATION

CONTENTS

1.0 Introduction

The MCS6532 is a multiple-function microprocessor support chip containing 128 bytes of RAM, sixteen I/O pins, an interval timer and an edge-sensitive interrupt input. It is designed to allow maximum flexibility in the implementation of systems which use the MCS6500 microcomputer components.

Some important features of the MCS6532 are:

* 8 bit bi-directional Data Bus for communication with the microprocessor
* Edge Sense Interrupt (Positive or Negative Edge Programmable)
* 128 x 8 static RAM
* Two 8 bit bi-directional data ports for interface to peripherals
* Two programmable Peripheral Data Direction Registers
* Programmable Interval Timer
* TTL & CMOS compatible peripheral lines
* Peripheral pins with Direct Transistor Drive Capability
* High Impedance Three-State Data Bus

2.0 MCS6532 Pinouts

Figure 2.1 shows the pin configuration for the MCS6532. These pins are described briefly in this section. A detailed description of the operation, and a specification of all AC and DC characteristics for these pins, is contained in subsequent sections.

PIN #	PIN NAME	DESCRIPTION
1, 20	VSS, GND	Chip power supply connections.
2-7, 40	AØ-A6	Address Inputs - Allow selection of the various RAM and I/O registers on the chip.
8-15	PAØ-PA7	Peripheral A I/O port. Eight-bit general-purpose bi-directional data port.
16-19, 21-24	PBØ-PB7	Peripheral B I/O port. Eight-bit general-purpose bi-directional data port.
25	IRQ	Interrupt Request Output. Goes to the processor IRQ or NMI input to allow interrupting.
26-33	DBØ-DB7	Data Bus - Allows transfer of 8 bit bytes of data between the processor and the MCS6532.
34	$\overline{RES}$	Reset - Clears all internal registers to zeros.
35	R/W	Read/Write control from processor.
36	$\overline{RS}$	RAM Select input.
37, 38	CS1, $\overline{CS2}$	Chip Select inputs.
39	Ø2	Phase Two system clock input.

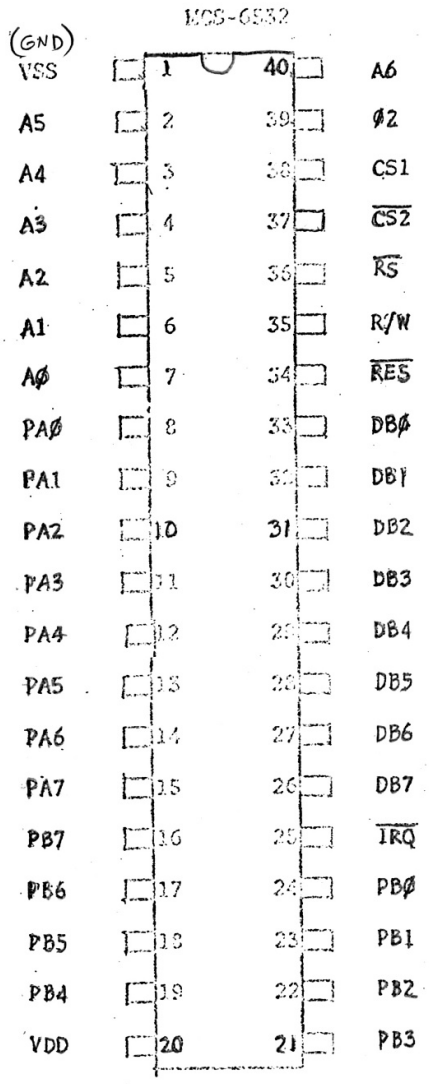


Figure 2.1 MOS 6532 PIN DESIGNATION

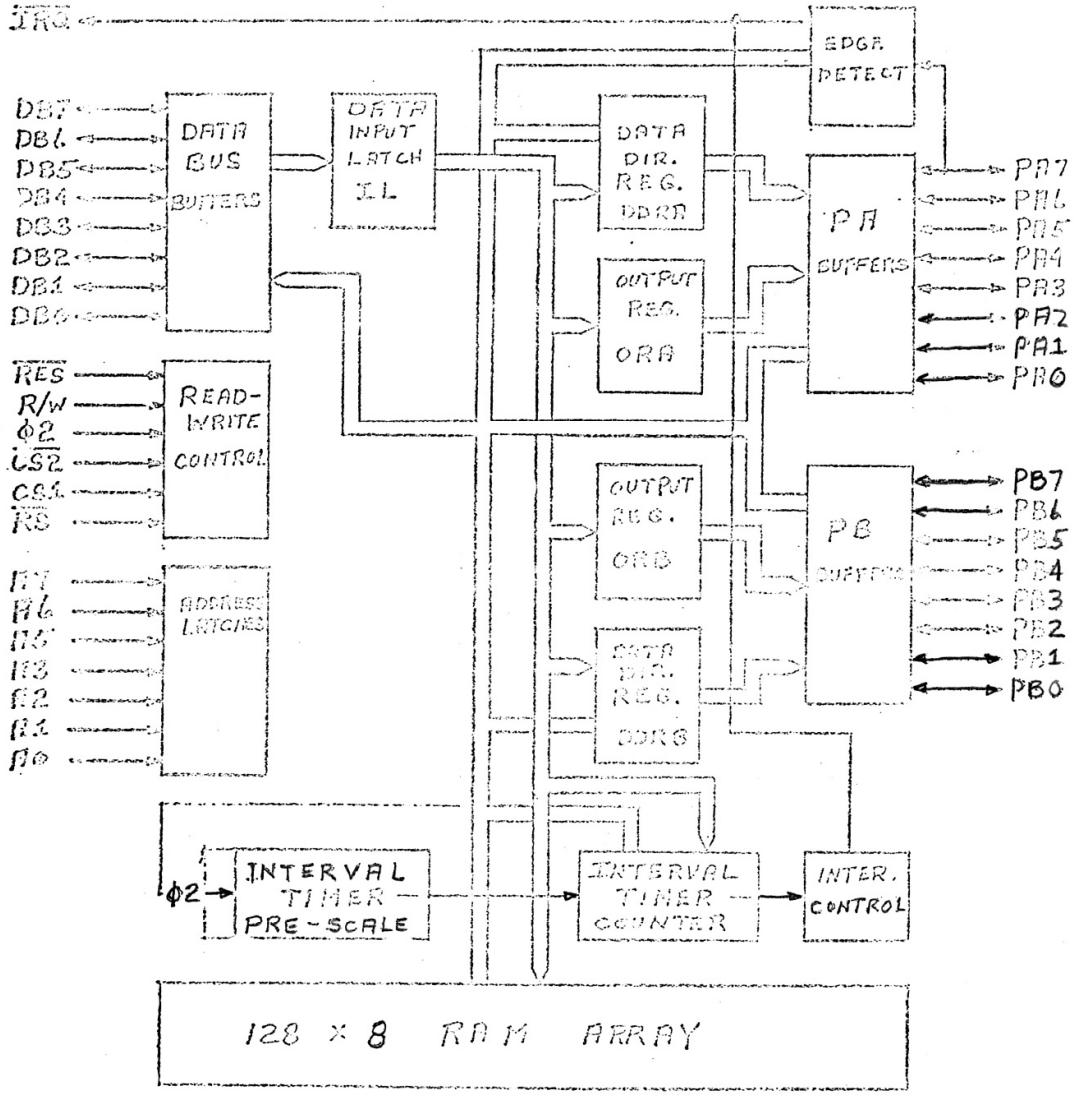


FIGURE 3.1. BLOCK DIAGRAM OF MCS6532

3.0 Internal Organization of the MCS6532

3.1 Introduction

Figure 3.1 contains a block diagram of the MCS6532 showing the various data paths, registers, buffers, etc. on the chip. These logic blocks are described in this section in sufficient detail to serve as a basis for the specifications contained in Sections 4.0, 5.0 and 6.0.

3.2 Data Bus Buffers

The buffers which drive the system data bus are push-pull devices which remain in the high-impedance state except when the MCS6532 is transferring data to the system processor. In the output mode, they are capable of driving one standard TTL device and up to ten MCS6500 family devices. In the input mode, the data bus pins represent primarily a capacitive load to the other devices in the system since the output drivers go to a high-impedance state.

3.3 Data Input Latch

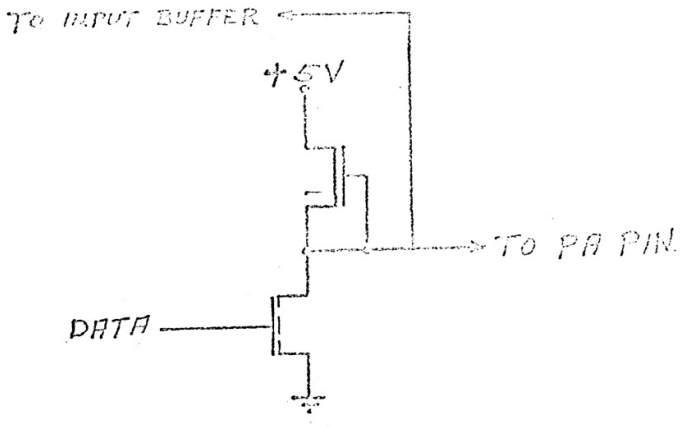
All data being transferred into the MCS6532 is first stored in the Data Input Latch. This is necessary in any I/O device to avoid "glitching" the peripheral output pins. The data is latched into the input latch during the Phase Two system clock pulse. From there it is transferred into the internal registers (RAM, DDRA, etc.) during the next Phase Two ($\phi 2$=0.4V) system clock pulse. This allows the peripheral interface output pins to remain stable except when they are going to reverse polarity.

3.4 Read/Write Control

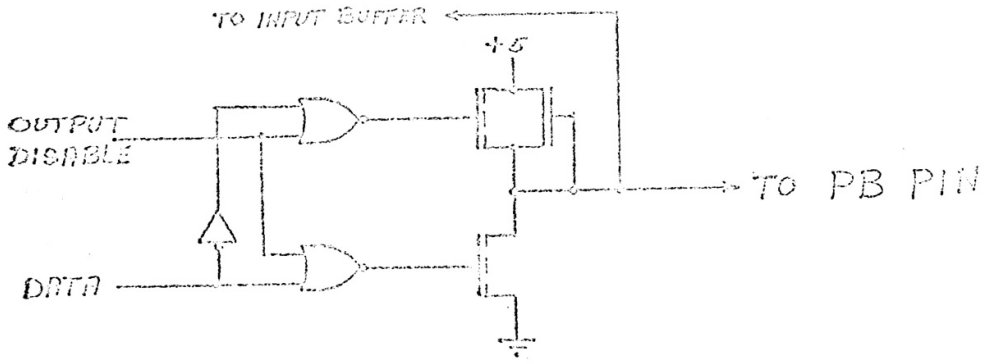
The Read/Write control logic responds to address inputs, chip select inputs, the R/W line and the clock input to control data transfers between the MCS6532 registers and the system data bus.

3.5 Address Latches

Since the data being transferred into the MCS6532 is first stored in the input latch and is transferred internally during the next Phase Two, it is necessary to latch the chip select and address inputs. The Address Latches store the addresses generated by the processor, latching the addresses on the leading edge of Phase Two. These addresses are then used to control the transfer of data from the Data Input Latch to the various registers on the chip.



PERIPHERAL A PORT BUFFER



PERIPHERAL B PORT BUFFER

FIGURE 3.2. MOS6532 PERIPHERAL BUFFERS

3.6 RAM Array

The Read/Write memory array can store up to 128 eight-bit bytes of data which can be written into the RAM by the system microprodessor. By providing the proper address and chip select signals, the processor can read the data at any time.

3.7 Peripheral Buffers

The peripheral buffers provide the voltage and current necessary for controlling peripheral devices. On the Peripheral A Port, the active pull-ups are always on and are always connected to the peripheral pin. For this reason, these pins represent one standard TTL load in the input mode. In the output mode, the buffers on both the PA and PB ports are capable of driving one standard TTL load. In addition, the PB buffers are capable of sourcing 3 ma at 1.5 VDC. This allows these pins to directly drive Darlington transistors.

Both the PA and the PB ports are capable of generating the voltage levels necessary to drive CMOS. However, the depletion-mode pull-up device which makes this possible causes both the PA and PB ports to source current in the input mode.

Figure 3.2 contains a logic diagram of the PA and PB Buffers.

3.8 Data Direction Registers

The PA and PB peripheral ports each consist of eight lines which can be individually programmed to act as either an input or an output. This input/output configuration is determined by the Data Direction Register. Setting a "0" into a bit of the Data Direction Register causes the corresponding peripheral pin to act as an input. A "1" causes the peripheral to act as an output.

3.9 Output Registers

As discussed in the previous section, the peripheral pins can be programmed to act as either an input or an output. In the output mode, the voltage on the peripheral pin is controlled by the corresponding bit of the Output Register. A "0" in Output Register causes the corresponding peripheral output line to go low (0.4V). A "1" causes the peripheral output line to go high (+5V).

3.10 Edge Detect Logic

In addition to acting as a peripheral I/O pin, PA7 can also act as an edge sensitive interrupt input. Any active transition of the signal on PA7 will set the internal interrupt flag. If the interrupt is enabled, the $\overline{IRQ}$ output will go low when the interrupt flag is set.

4.0 Microprocessor Interface

The interface between the MCS6532 and the system microprocessor contains signals for transferring data (DB0-DB7), for controlling the direction and timing of these transfers (R/$\overline{W}$, ϕ2), for addressing the various on-chip registers (A0-A6, $\overline{RS}$, CS1, $\overline{CS2}$), for resetting the chip ($\overline{RES}$) and for allowing the MCS6532 to interrupt the microprocessor ($\overline{IRQ}$). The operation of each of these is described in detail in this section.

4.1 Resetting the MCS6532

All of the registers on the MCS6532 (excluding the RAM) can be reset to logic zero by placing a low (0.4V) on the $\overline{RES}$ input. This is normally accomplished by connecting this input to the system reset signal. As long as $\overline{RES}$ is low, all peripheral I/O pins will be set to input state and all interrupts will be disabled. Causing $\overline{RES}$ to go high will allow all normal chip operations to begin.

4.2 Interrupting the Microprocessor

The MCS6532 can interrupt the microprocessor as a result of an active transition on the edge-sensitive input or from a time-out of the interval timer. Either of these conditions can cause the $\overline{IRQ}$ output to go low to interrupt the processor. This $\overline{IRQ}$ output is "open-drain", i.e., it has no pull-up device. This allows this signal to be "wire-or'ed" with similar signals from other peripheral interface devices in the system.

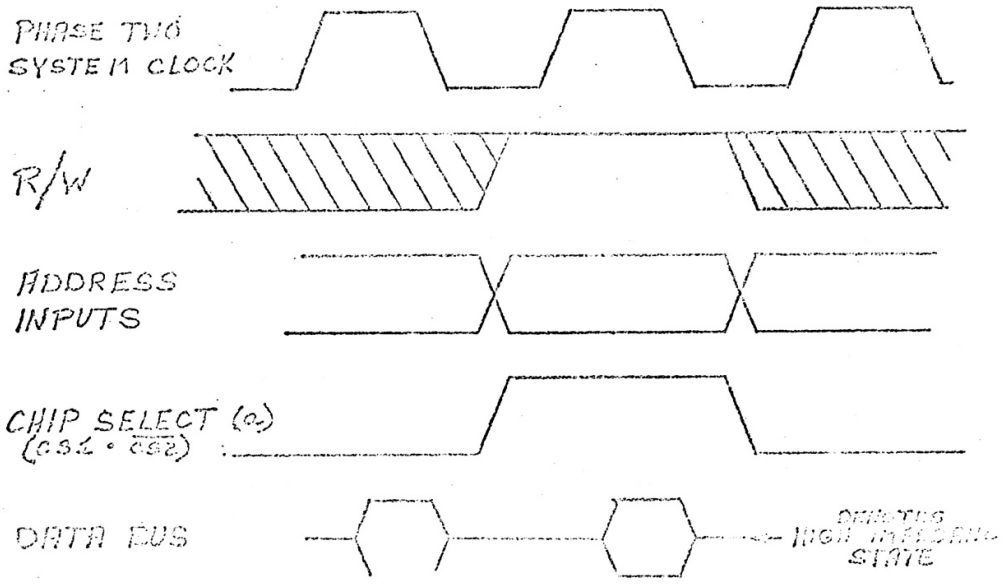
4.3 Reading the MCS6532

Data can be transferred from the MCS6532 into the system microprocessor by placing a logic 1 on the R/W line, selecting the chip (CS1=1, $\overline{CS2}$=0) and placing the address of the desired data on the address inputs (A0-A6, $\overline{RS}$). The desired data will then be placed on the Data Bus during the Phase Two system clock pulse (ϕ2=2.4V). This timing sequence is shown in Figure 4.1.

Selection of the various I/O ports, registers and RAM bytes is accomplished by connecting the microprocessor address outputs to the RAM Select input ($\overline{RS}$), the chip select inputs (CS1, $\overline{CS2}$) and the address inputs (A0-A6). The RAM is selected by placing a low (0.4V) on $\overline{RS}$ and selecting the chip. The address inputs (A0-A6) can then be used to select one of the 128 bytes of memory in the RAM section. With the $\overline{RS}$ input high and the chip selected (CS1=2.4V, $\overline{CS2}$=0.4V), the address inputs can be used to address the various I/O registers as shown in Figure 4.2.

4.4 Writing the MCS6532

Writing from the microprocessor into the MCS6532 registers, RAM memory, etc. is accomplished in much the same manner as that described in the previous section for reading. However, the R/W line must go low to cause the transfer of data into the chip. With the chip selected, and R/W=0.4V, the data on the Data Bus will be transferred into the input latch and then into the selected I/O register or RAM memory location. This timing sequence is shown in Figure 4.3. As shown in Figure 4.2, addressing of the I/O registers operates somewhat differently for reading and writing.



NOTES

(a) CHIP SELECT = CS1 • $\overline{CS2}$

FIGURE 4.1. MCS 6532 READ SEQUENCE

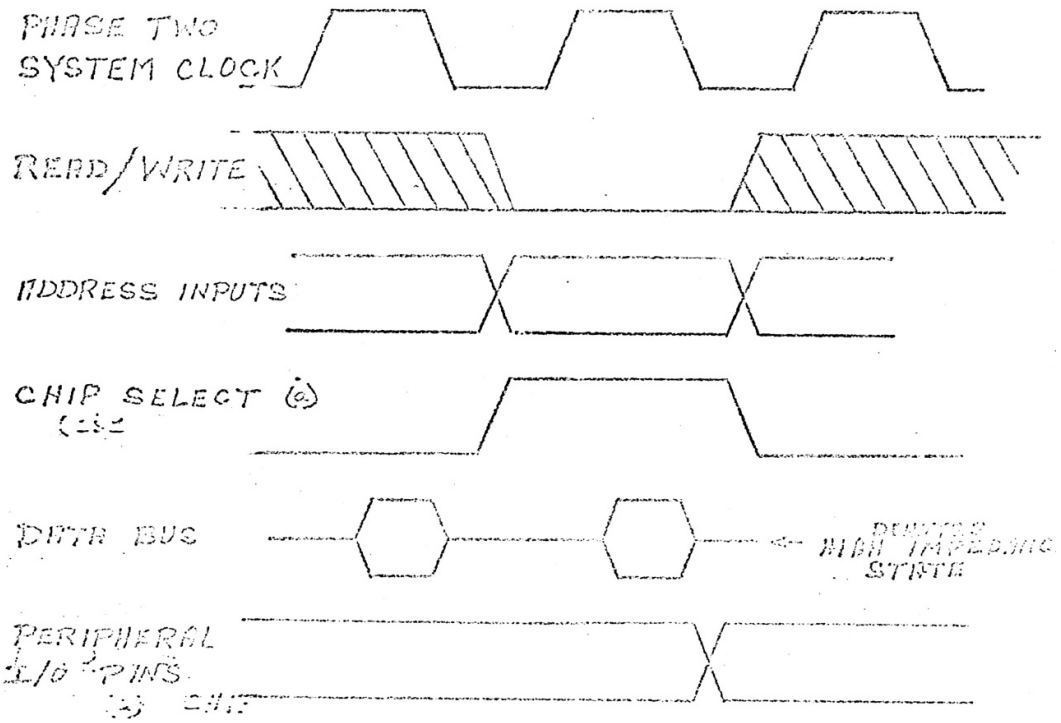
	$\overline{RS}$	R/W	A4	A3	A2	A1	A0
Read PA Pins	1	1	X	X	0	0	0
Write Output Register A	1	0	X	X	0	0	0
Read Data Direction Register A	1	1	X	X	0	0	1
Write Data Direction Register A	1	0	X	X	0	0	1
Read Output Register B	1	1	X	X	0	1	0
Write Output Register B	1	0	X	X	0	1	0
Read Data Direction Register B	1	1	X	X	0	1	1
Write Data Direction Register B	1	0	X	X	0	1	1
Read Interval Timer	1	1	X	(b)	1	X	0
Write Interval Timer							
÷ 1	1	0	1	(b)	1	0	0
÷ 8	1	0	1	(b)	1	0	1
÷ 64	1	0	1	(b)	1	1	0
÷ 1024	1	0	1	(b)	1	1	1
Read Interrupt Flags	1	1	X	X	1	X	1
Write Edge Detect Control	1	0	0	X	1	(c)	(d)

NOTES:

(a) X = Don't Care
(b) A3 = 0, Disable Interrupt to $\overline{IRQ}$ from Timer
A3 = 1, Enable Interrupt to $\overline{IRQ}$ from Timer
(c) A1 = 0, Disable Interrupt to $\overline{IRQ}$ from PA7
A1 = 1, Enable Interrupt to $\overline{IRQ}$ from PA7
(d) A0 = 0, Negative Edge Detect
A0 = 1, Positive Edge Detect
(e) 0 = 0.4V
1 = 2.4V
(f) CS1 = 1, $\overline{CS2}$ = 0

Bit 7 = flag goes high on interval time-out
Bit 6 = flag goes high on active transition

Figure 4.2 Addressing the MCS6532 Registers



NOTES

(a) CHIP SELECT = $CS1 \cdot \overline{CS2}$

FIGURE 4.3. MCS6532 WRITE SEQUENCE

5.0 Peripheral A Interface

The Peripheral A I/O port consists of eight lines which can be individually programmed to act as either an input or an output. A logic zero in a bit of the Data Direction Register (DDRA) causes the corresponding line of the PA port to act as an input. A logic one causes the corresponding PA line to act as an output. The voltage on any line programmed to be an output is determined by the corresponding bit in the Output Register (ORA).

Data is read directly from the PA pins during any read operation. For any output pin, the data transferred into the processor will be the same as that contained in the Output Register if the voltage on the pin is allowed to go to 2.4V for a logic one. Note that for input lines, the processor can write into the corresponding bit of the Output Register. This will not effect the polarity on the pin until the corresponding bit of DDRA is set to a logic one to allow the peripheral pin to act as an output.

Figure 4.3 shows the timing sequence for writing the Peripheral port. Note that the outputs change on Phase Two (Phase Two=0.4V) as discussed in Section 3.3.

In addition to acting as a peripheral I/O line, the PA7 line can be used as an edge-detecting input. In this mode, an active transition will set the internal interrupt flag (bit 6 of the Interrupt Flag register). Setting the interrupt flag will cause $\overline{IRQ}$ output to go low if the PA7 interrupt has been enabled.

Control of the PA7 edge detecting mode is accomplished by writing to one of four address. In this operation, A0 controls the polarity of the active transition and A1 acts to enable or disable interrupting of the processor. The data which is placed on the Data Bus during this operation is discarded and has no effect on the control of PA7.

Setting of the PA7 active transition if the pin is being used as a normal input or as a peripheral control output. The flag will also be set by an active transition if interrupting from PA7 is disabled. The reset signal ($\overline{RES}$) will disable the PA7 interrupt and will set the active transition to negative (high to low). During the system initialization routine, it is possible to set the interrupt flag by a negative transition. It may also be set by changing the polarity of the active interrupt. It is therefore recommended that the interrupt flag be cleared before enabling interrupting from PA7.

Clearing of the PA7 Interrupt Flag occurs when the microprocessor reads the Interrupt Flag Register as shown in Figure 4.2.

6.0 Peripheral B Interface

The operation of the Peripheral B Input/Output port is exactly the same as the normal I/O operation of the Peripheral A port. The eight lines can each be programmed to act as either an input or as an output by placing a 0 or a 1 into the Data Direction register (DDRB). In the output mode, the voltage on a peripheral pin in controlled by the Output Register (ORB).

The primary difference between the PA and the PB ports is in the operation of the output buffers which drive these pins. As shown in Figure 3.2, the buffers are push-pull devices which are capable of sourcing 3 ma at 1.5 volts. This allows these pins to directly drive transistor switches. To assure that the microprocessor will read proper data on a "Read PB" operation, sufficient logic is provided in the chip to allow the microprocessor to read the Output Register instead of reading the peripheral pin as on the PA port. The AC and DC specifications for the PB port are contained in Sections 10.0 and 11.0.

7.0 RAM Operation

The 128 x 8 Read/Write memory acts as a conventional static RAM. Data can be written into the RAM from the microprocessor by selecting the chip (CS1=1, $\overline{CS2}$=Ø) and by setting $\overline{RS}$ to a logic Ø (0.4V). Address lines AØ through A6 are then used to select the desired byte of storage. The timing for the Read and Write operations is specified in detail in Sections 10.0 and 11.0.

8.0 Interval Timer Operation

8.1 Introduction

The interval timer in the MCS6532 is a duplicate of that provided on the MCS6530. This counter is divided into two sections; a pre-scale counter and a programmable counter. In addition, the interval timer has interrupt and control logic which determines the operating modes in the timer. Figure 8.1 shows a detailed block diagram of the Interval Timer.

8.2 Pre-scale Counter

The 10 bit pre-scale counter generates a pulse every 1, 8, 64 or 1024 system clock pulses. The pulses from the pre-scale are then counted in the programmable counter. Selection of this pre-scale frequency is controlled by varying the address used when writing into the programmable counter. The four addresses which can be used when writing into the interval timer are shown in Figure 4.2 along with the associated pre-scale frequency.

8.3 Programmable Counter

The programmable portion of the Interval Timer consists of an eight-bit decrementing counter. This counter can be preset to any desired number by writing from the microprocessor into one of the eight addresses assigned to the counter. The address selected will determine the pre-scale counter output frequency and, in addition, will control the $\overline{IRQ}$ output.

Immediately after the write operation is complete, the counter will begin to decrement at a frequency determined by the selected pre-scale. When the programmable portion of the interval timer decrements to zero, the interrupt flag will be set. On the next $\phi 2$, the $\overline{IRQ}$ output will go low if the interrupt was enabled during the Timer Write operation (A3=1). At this time the counter will begin to decrement at the system clock rate. This allows the processor to read the counter to determine the "time since interrupt" to a maximum of 255 clock cycles.

The status of the interval timer flag can be determined by reading bit 7 in the Interrupt Flag Register. A logic 1 indicates that the flag is set by a time-out. A logic ϕ indicates that the flag has been cleared.

Figure 8.2 shows the timing sequence which takes place in the MCS6532 interval timer.

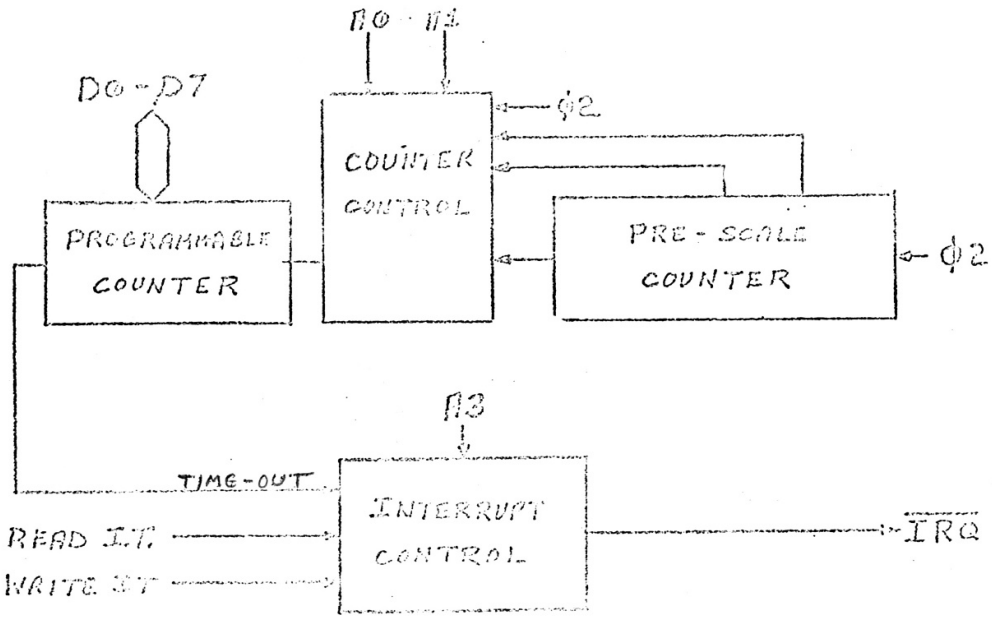
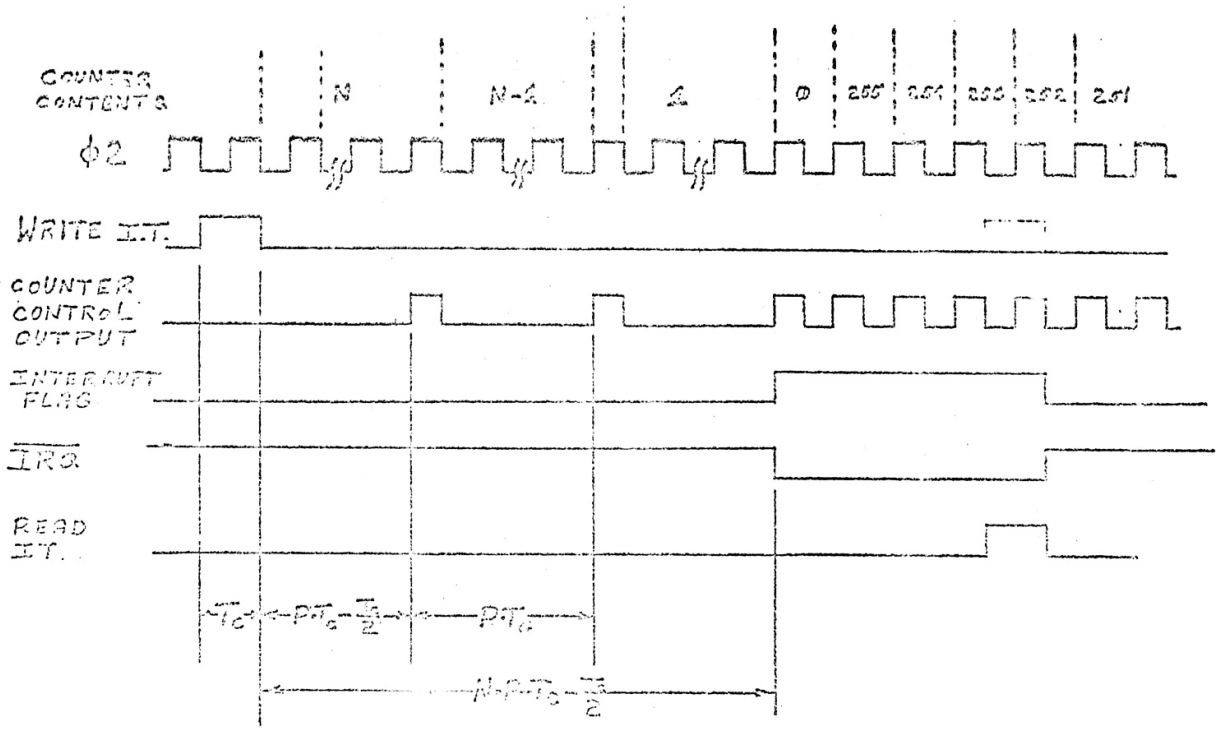


FIGURE 9.1. BLOCK DIAGRAM OF INTERVAL TIMER



NOTES:

P = PRE-SCALE (1, 8, 64 OR 1024)

T_c = CLOCK PERIOD

N = NUMBER LOADED INTO TIMER FROM PROCESSOR

FIGURE 8.2. INTERVAL TIMER TIMING

9.0 Programming the MCS6532

9.1 Introduction

There are several very important considerations in the programming of the MCS6532 Interval Timer, and edge-detecting inputs. These are discussed in detail in this section.

9.2 Identification of the MCS6532 Registers for the Assembler.

Because several very important operations in the MCS6532 are controlled by varying addresses, it is usually recommended that each of these addresses be given a separate and meaningful label at the beginning of the program. This will minimize the probability of errors in the text of the program. This can be accomplished very effectively as shown in Figure 9.1.

9.3 Programming the Interval Timer

As described in Section 8, the interval timer can be operated either through the processor interrupt or by polling the interrupt flag to detect the time-out. Each of these modes is discussed separately below.

9.3.1 Polled Interval Timer Operation

Operation of the interval timer in the polled mode requires that the processor first load the timer for the proper time-out period. The processor then goes into a software loop in which the timer flag is constantly tested. This sequence is shown in Figure 9.2. In the example shown, a peripheral output is set low for a period determined by the timer.

9.3.2 Operation of the Timer through the Processor Interrupt

By using the proper address during the Timer Write operation, the $\overline{IRQ}$ output can be used to signal the processor that a time-out has occurred. In this operation, the timer is loaded with the proper data during execution of the main-line program and the Interrupt Service routine is used to respond to the time-out. This operation is shown in Figure 9.3. In this example a peripheral output is set low for a period of time determined by the interval timer.

Note that the interrupt service routine contains the instructions necessary to disable subsequent interrupts from the timer. This is necessary in any operation where only a single timer interrupt is desired.

Figure 9.4 shows a similar example where the timer is used to generate a square wave on a peripheral pin. In this mode, the timer is re-loaded during the interrupt service routine to enable generation of the next interrupt in the sequence.

9.4 Correction of the Time-Out Period

Very accurate time periods can be generated by a microprocessor using the interval timer if the necessary software is provided to take advantage of the "time-since-interrupt" feature of the MCS6532 interval timer. After a time-out has occurred, the interval timer will continue to decrement at the system clock rate. The "time-since-interrupt" can then be determined by reading the contents of the timer counter. This data can then be used to adjust the next time-out to maintain very accurate overall frequency. Figure 9.5 contains an example of a program which generates pulses which are very accurate in frequency.

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```
LINE # LOC      CODE        LINE

0001   0000                 *  =$A000
0002   A000                 PADAT32 *=*+1 PA OUTPUT REG
0003   A001                 PADIR32 *=*+1 PA DATA DIR REG
0004   A002                 PBDAT32 *=*+1 PB OUTPUT REG
0005   A003                 PBDIR32 *=*+1 PB DATA DIR REG
0006   A004                 RITD32  =* READ INT TIMER
0007   A004                 EDND32  *=*+1 EDGE DET-NEG DIS
0008   A005                 EDPD32  =* EDGE DET-POS DIS
0009   A005                 RDIF32  *=*+1 READ INT FLAG
0010   A006                 EDNE32  *=*+1 EDGE DET-NEG EN
0011   A007                 EDPE32  *=*+13 EDGE DET-POS EN
0012   A014                 IT1D32  *=*+1 T-DIV 1;NO INT
0013   A015                 IT8D32  *=*+1 I T-DIV 8;NO INT
0014   A016                 IT6D32  *=*+1 I T-DIV 64;NO INT
0015   A017                 ITKD32  *=*+5 IT-DIV 1024;NO INT
0016   A01C                 IT1E32  *=*+1 IT-DIV  ;INT EN
0017   A01D                 IT8E32  *=*+1 IT-DIV 64;INT EN
0018   A01E                 IT6F32  *=*+1 IT-DIV 64;INT EN
0019   A01F                 ITKE32  *=*+1 IT-DIV 1024;INT EN
0020   A020                 .END

ERRORS = 0000 WARNINGS = 0000

 SYMBOL VALUE

 PADAT32   A000
 PADIR32   A001
 PBDAT32   A002
 PBDIR32   A003
 RITD32    A004
 EDND32    A004
 EDPD32    A005
 RDIF32    A005
 EDNE32    A006
 EDPE32    A007
 IT1D32    A014
 IT8D32    A015
 IT6D32    A016
 ITKD32    A017
 IT1E32    A01C
 IT8E32    A01D
 IT6E32    A01E
 ITKE32    A01F
END OF ASSEMBLY
```

10.0 D.C. Specifications

This section contains the static operating voltages and currents for the MCS6532. These specifications shall apply over the operating temperature range of 25°C unless otherwise noted.

10.1 Maximum Ratings

RATING	SYMBOL	VOLTAGE	UNIT
Supply Voltage	V_{CC}	-.3 to +7.0	V
Input/Output Voltage	V_{IN}	-.3 to +7.0	V
Operating Temperature Range	T_{OP}	0 to 70	°C
Storage Temperature Range	T_{STC}	-55 to +150	°C

All inputs contain protection circuitry to prevent damage due to high static charges. Care should be exercised to prevent unnecessary application of voltage outside the specification range.

10.2 Static Operating Characteristics

ELECTRICAL CHARACTERISTICS (VCC = 5.0V ± 5%, VSS = 0V

CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNIT
Input High Voltage	V_{IH}	V_{SS} + 2.4		VCC	V
Input Low Voltage	V_{IL}	V_{SS} - .3		V_{SS} + .4	V
Input Leakage Current; V_{IN} = 0 to 5V A0-A6, RS, R/W, RESET, Ø2, CS1, CS2	I_{IN}		1.0	2.5	uA
Input Leakage Current for High Impedence State (Three State); V_{IN} = .4V to 2.4V; DBØ-DB7	ITSI		±1.0	+10.0	uA
Input High Current; V_{IH} = 2.4V PAØ-PA7, PBØ-PB7	I_{IH}	-100.	-300		uA
Input Low Current; V_{IL} = .4V PAØ-PA7, PBØ-PB7			-1.0	-1.6	MA
Output Voltage Low V_{CC} = MIN, I_{LOAD} 1.6 ma					
Output High Voltage V_{CC} = MIN, I_{LOAD} -100uA I_{LOAD} -3 MA PBØ-PB7	V_{OH}	V_{SS} + 2.4 V_{SS} + 1.5			
Output High Current (Sourcing); PBØ-PB7 V_{OH} = 2.4V .- 1.5V Available for other than TTL (Darlingtons)	I_{OH}	-100 -3.0	-1000 -5.0		uA MA
Output Low Current (Sinking); VOL .4V	I_{OL}	1.6			MA
Clock Input Capacitance	C_{CLK}			30	pf
Input Capacitance	C_{IN}			10	pf
Output Capacitance	C_{OUT}			10	PF
Power Dissipation	P_D		500	1000	MW

All values are D.C. readings.

11.0 A.C. Specifications

This section contains the dynamic operating characteristics for the MCS6532. These specifications apply at 25°C unless otherwise noted.

11.1 Read Operation

Figure 11.1 shows the timing sequence for the MCS6532 Read operation. This figure also identifies the dynamic parameters which will be specified in this section.

The limits for these parameters are:

CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNIT
R/W valid before positive transition of clock	TWCR	180			NS
Address valid before positive transition of clock	TACR	180			NS
Peripheral data valid before positive transition of clock	TPCR	300			NS
Data Bus valid after positive transition of clock	TCDR			535	NS
Data Bus Hold Time	TDR	10			NS
$\overline{IRQ}$ (Interval Timer Interrupt) valid before positive transition of clock	TIC	200			NS

Loading = 30 pf + TTL load for PA0-PA7, PB0-PB7

=130 pf + 1 TTL load for D0-D7

11.3 Write Operation

Figure 11.2 shows the timing sequence for a MCS6532 Write operation. This figure also identifies the dynamic parameters which will be specified in this section.

CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNIT
Clock Period	T_{CYC}	1			uS
Rise & Fall Times	TR, TF			25	NS
Clock Pulse Width	TC	470			NS
R/W valid before positive transition of clock	TWCW	180			NS
Address valid before positive transition of clock	TACW	180			NS
Data Bus valid before negative transition of clock	TDCW	300			NS
Data Bus Hold Time	THW	10			NS
Peripheral Data valid after negative transition of clock	TCTW			1	uS
Peripheral Data valid after negative transition of clock driving CMOS (Level = VCC-30%)	TCMOS			2	uS

11.3 Write Operation

Figure 11.2 shows the timing sequence for a MCS6532 Write operation. This figure also identifies the dynamic parameters which will be specified in this section.

CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNIT
Clock Period	T_{CYC}	1			uS
Rise & Fall Times	TR, TF			25	NS
Clock Pulse Width	TC	470			NS
R/W valid before positive transition of clock	TWCW	180			NS
Address valid before positive transition of clock	TACW	180			NS
Data Bus valid before negative transition of clock	TDCW	300			NS
Data Bus Hold Time	THW	10			NS
Peripheral Data valid after negative transition of clock	TCPW			1	uS
Peripheral Data valid after negative transition of clock driving CMOS (Level = VCC-30%)	TCMOS			2	uS